Zynq UltraScale+™ RFSoC Product Overview

Mete YASAN
Breakthrough FPGA & SoC Architecture at 16nm
UltraScale+ Portfolio Highlights

FPGAs

• Up to 3X performance/watt fabric
• Up to 33 Gb/s Transceivers
• 2.5X DSP bandwidth
• PCIe Gen3 x16 and Gen4 x8
• 2,666Mb/s DDR4

1: Compared to 28nm 7 Series FPGAs

MPSoCs

• 64-Bit ARM Quad Core Cortex-A53
• 32-bit ARM Dual Core Cortex-R5 Real Time
• ARM Mali-400MP2 GPU (2D/3D Displays)
• Integrated DDR4 Memory Controller
• Block-Level, Granular Power Management
The First RFSoC

✓ Integrated RF-Class Analog and Error Correction Technology

✓ Delivering 50-75% Power & Footprint Reduction

✓ Full Programmability Across the RF Signal Chain
Part of a Complete System Based on Production-Proven MPSoCs
Monolithically Integrated

Processing System
- Quad-Core A53 (64-bit)
- Dual-Core R5 (32-bit)

Hardened Engines
- PCIe Gen3 & Gen4
- 100G Cores

33G Transceivers
- 33Gb/s
- 28G Backplane Capable

ADC
Analog-to-Digital Converters
Up to 4 GSPS

DAC
Digital-to-Analog Converters
Up to 6.4 GSPS

Soft Decision Forward Error Correction
LDPC & Turbo Support

Programmable Logic
- 16nm FinFET
- UltraScale+ FPGA Fabric

DSP-Intensive
- 4,272 DSP slices
- 7,612 GMACs

33G Transceivers
- 33Gb/s
- 28G Backplane Capable
Integrated Direct-RF Data Converters
Advantages of Integrated Direct-RF Converters

Reduced System Power
- Reduces data converter power
- Eliminates FPGA-to-Analog interface power

Dramatic System Footprint Reduction
- Eliminates discrete converters
- Enables scalability for increasing channel count

Shorter Design Cycle
- Simplified system design with fewer components
- Eliminates JES204B/C analog interface design

Direct RF Sampling for Platform Flexibility
- RF-design moved to the digital domain for full programmability
- Reduces & minimizes analog signal processing components
RF-Analog Execution: Years in the Making

28nm Test Chip Designed & Validated

2012

Integrated ADC & DAC with Virtex®-7 FPGA

Test Chip Designed & Validated

2016

Integrated ADC & DAC in 16nm FinFET

Product Shipped to Multiple Customers

2017

12-bit 4 GSPS ADCs
14-bit 6.4 GSPS DACs
Power Reduction in 2x2 RF Interface

SoC
- Processing System
- Digital Design
- Transceivers
  - 1 Watt
  - JESD204 Converter Interface IP
  - Transceivers
  - 1 Watt
  - JESD204 Converter Interface IP
  - Transceivers
- Transceivers
  - 2.25 Watts
  - ADC
  - 1.75 Watts
  - DAC
  - 2.25 Watts
  - ADC
  - 1.75 Watts
  - DAC

RFSocC
- Processing System
- Digital Design
- Transceivers
  - 1.3W
  - ADC
  - 1W
  - DAC

10 Watts
- 2 Watts JESD + 8W Converters

2.3 Watts
# Power Savings in Radio1 Digital Front-End with an Integrated Data Converter Subsystem

<table>
<thead>
<tr>
<th>Discrete Implementation</th>
<th>4x4 100MHz</th>
<th>4x4 200MHz</th>
<th>8x8 100MHz</th>
</tr>
</thead>
<tbody>
<tr>
<td>Programmable Device</td>
<td>15W</td>
<td>23W</td>
<td>23W</td>
</tr>
<tr>
<td>RF ADC/DAC Components</td>
<td>16W</td>
<td>16W</td>
<td>32W</td>
</tr>
<tr>
<td>Total Power of Discrete Implementation</td>
<td>31W</td>
<td>39W</td>
<td>55W</td>
</tr>
</tbody>
</table>

| Integrated RF-Analog Implementation         |             |            |            |
| Programmable Device + DC Subsystem          | 18W         | 25W        | 27W        |
| **TOTAL POWER SAVINGS**                     | **13W**     | **14W**    | **28W**    |

↓ 41%   ↓ 37%   ↓ 51%

1: With Digital Pre-Distortion (DPD) Implementation
Footprint Reduction: 4x4 (Single Channel RFICs)

~56%¹ Footprint Reduction

¹: Based on commercially available devices of similar performance
Footprint Reduction: Integrating 8Rx 8Tx Channels Replacing Four-Channel RF-Sampling ADCs/DACs

34% Footprint Reduction

~30mm x 30mm

4X (15mm x 15mm)

~35mm x 35mm
Reducing Design Cycle

- Eliminates JESD204B
- Simplifies Board Design
- Enables System Scalability

Virtex® UltraScale™ VU35P

Role
IPSec, SSL, Firewall, GZIP, OSV, SHA

VHBM Controller
PCIe/CCIX

400GE MAC

NIC w/Half the Height & Length

All Programmable Device

1.75 Watts

2.25 Watts

1.75 Watts

1 Watt

JESD204 Converter Interface IP

Transceivers

ADC

DAC
## Integrated Direct-RF Data Converters for Platform Flexibility

<table>
<thead>
<tr>
<th>Feature</th>
<th>Benefit</th>
</tr>
</thead>
<tbody>
<tr>
<td>4GSPs or 2GSPS ADCs with 12-bit Resolution 6.4GSPS DACs with 14-bit Resolution</td>
<td>• 4GHz of direct-RF bandwidth</td>
</tr>
<tr>
<td>RF-Sampling with Full DSP Subsystem</td>
<td>• RF-design in programmable digital domain, reducing external analog components  &lt;br&gt; • Full Digital Down-Conversion (DDC) and Up-Conversion (DUC)  &lt;br&gt; • Optionally bypass subsystem to programmable logic for custom mixing &amp; filtering</td>
</tr>
<tr>
<td>Based on 16nm FinFET+</td>
<td>• Optimal performance-per-watt and at least two process nodes ahead of latest generation discrete components</td>
</tr>
<tr>
<td>Dedicated Communication-Grade PLLs</td>
<td>• Leverage lower frequency external clock to drive high speed converters</td>
</tr>
<tr>
<td>Multi-Band Support</td>
<td>• Enable flexible carrier aggregation through a single RF signal chain</td>
</tr>
</tbody>
</table>

### Diagram

- **Programmable Logic**
  - DSP-Based Mixing & Filtering
  - 4GSPS ADCs
  - 6.4GSPS DACs

- **Full DSP Subsystem on 16nm**
  - RF Sampling
  - Multi-Band Support

- **Low Frequency External Clock**
  - Band 1
  - Band 2

- **Optionally bypass subsystem**

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Platform Flexibility with Direct RF-Sampling

Traditional IF (Intermediate Frequency) Sampling
Signal conditioning before ADC Sampling using analog components

- Power efficient
- Greater footprint due to multiple components
- Greater design effort due to BOM complexity
- Limited flexibility due to fixed components
Signal Processing Integration from RF Front-End to Digital Front-End

**DSP Mixing and Filtering**
- 6 TeraMACs of DSP bandwidth
- Digital Up-Conversion and Down-Conversion

- Gain/Phase Compensation
- IQ Mixers
- NCO

- Decimation
- Interpolation

**4GHz of Direct-RF Bandwidth**
- Eight 4GSPS ADCs, or Sixteen 2GSPS ADCs
- Eight or Sixteen 6.4GSPS DACs

**Flexibility to Bypass Subsystem**
- Optionally bypass subsystem for fully custom signal conditioning
- Not possible with discrete converters (I/O limitation)

**Communication-Grade PLLs**
Utilize lower frequency on-board clocks
Multi-Band Support in the Digital Domain for Carrier Aggregation

<table>
<thead>
<tr>
<th>Analog (manually design and adjust multiple RF signal chains)</th>
<th>Digital</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Complex</strong> RF Signal Chains</td>
<td>DSP</td>
</tr>
<tr>
<td>Multi-Band</td>
<td></td>
</tr>
<tr>
<td>Band 1</td>
<td></td>
</tr>
<tr>
<td>Band 2</td>
<td></td>
</tr>
<tr>
<td><strong>Simplified</strong> RF Signal Chain</td>
<td></td>
</tr>
<tr>
<td><strong>Analog</strong> (digitally program each RF chain per carrier)</td>
<td><strong>Digital</strong></td>
</tr>
<tr>
<td><strong>Fixed Discrete Components</strong></td>
<td>DSP</td>
</tr>
</tbody>
</table>

Multiple PCBs and Configurations for Different Channel Aggregations

Single Platform Multi-Band Reconfigurable
Preliminary RFSoC ADC Results
Band 42, 2-tone FIN ~ 3.5GHz @ -26dBFS, FS=4GS/s

> High performance at low signal amplitude
> Band 42 (5G) performance optimization validated – aliased in 1st Nyquist Zone
Integrated Soft-Decision FEC
Xilinx FEC Codec Experience for Communications

20 Years of Providing Soft FEC IP
- Backhaul / Storage LDPC
- 3GPP Turbo Encoder
- Reed-Solomon Encoder
- Viterbi Decoder
- Convolutional Encoder
- Reed-Solomon Decoder

Hard RS-FEC in UltraScale+ FPGAs & MPSoCs
Error Correction over Electrical & Optical Interconnect

Integrated SD-FEC Blocks in Zynq UltraScale+ RFSoCs
BER Injection & Error Correction using LDPC codes
Advantages of Integrated SD-FEC in RFSoC

**High Throughput**
- High performance core with LPDC and Turbo code support
- Low Latency

**Flexible LDPC Code Construction & Design Integration**
- Supports industry standard codes (WiFi, 3GPP, DOCSIS, Verizon 5G)
- Programmability for proprietary codes

**Reduced System Power**
- Hardened 16nm FinFET silicon vs. soft implementation in FPGA fabric
- Enables compliance with stringent thermal requirements
**High Throughput and Compute Bandwidth**

**High Performance Core and Interface**
- 667MHz $F_{\text{MAX}}$ for high throughput system design
- Unachievable in a soft core

**High LDPC Throughput**
- Up to 21 Gb/s encode per core
- Up to 2.67 Gb/s decode per core @8 iterations

**Flexible Bus Interface**
Allow compatible $F_{\text{MAX}}$ in FPGA fabric

**Turbo Decode**
- Up to 1.78Gb/s per core @6 iterations
- 4G LTE-Advanced, 4G LTE-Advanced Pro

**Diagram Details**
- SD-FEC
- Core Clock 667MHz
- CDC & Bus Width Conv. (AXI)
- Shared Memory Subsystem
- LDPC Encoder/Decoder
- Turbo Decoder
- Pipelined Interface
- $D_{\text{in}}$ 1x 512b, 2x 256b, 4x 128b
- Flexible Bus-Width
Flexible Integration & Robust Coding Schemes

Flexible Code Construction
- Support for rate-compatible custom codes
- Multi-level LDPC code support

Optional Soft Output
- 8-bit soft LLR
- For further decoding or modulation

Flexible AXI Interfacing
- AXI-Interface to ease integration
- Supports different word lengths
- Supports out-of-order execution

Flexible # of Iterations
- Match compute effort to requirements
- Programmable up to 64 Iterations
- Supports early termination

Programmable Logic

SD-FEC
- AXI Based INTF
- LDPC Encoder/Decoder
- Shared Memory Subsystem
- Turbo Decoder

Pipelined Interface

Parameters or Custom Codes

LLR in Fabric
(Log Likelihood Ratio)
Dramatic Power Reduction vs. Soft Core
Example of LDPC Integrated Core at 2Gb/s Throughput

LDPC FEC Soft Cores
~1M System Logic Cells (425K LUTs)

- 33% Logic of Device

LDPC #1  LDPC #2

Processing System

~6.4W of Dynamic Power\(^1\)

Integrated SD-FEC

~1.2W of Dynamic Power
1 TeraOPS/core

- No additional resources required
- 6-10X lower latency vs. soft core

\(^1\): 258 Block RAMs (BRAM36k)

- 150k LUTs
- 9.3Mbits\(^1\) for storage & buffering
Excellent SD-FEC Hardware Results

Close Match Between Golden Double-Precision Floating-Point Model and Hardware Implementation

- 256 QAM, DOCSIS, rate = 0.85
- 1024 QAM, DOCSIS, rate = 0.75

3.5Gb/s Throughput
Comprehensive Solution of Tools, IP, and Evaluation Platforms

Tools

VIVADO® HLx Editions
IP Integrator
SDK
SDx™ Environments
System Generator
MATLAB & SIMULINK
Complete Solution

IP Portfolio
FEC Codes
5G New Radio*
3GPP Baseband
DPD
DOCSIS 3.x

Evaluation Platforms

*Under Development
Zynq UltraScale+ RFSoC Roadmap and Product Families

Mete YASAN
FAE
Integrated RF Data Converter Family Roadmap

1st Generation
ZU2XDR

Maximum RF Input Frequency = 4GHz
• 8 or 16 DACs @ 6.544GSPS
• 8 ADCs @ 4.096GSPS or 16 ADCs @ 2.058GSPS

2nd Generation
ZU3XDR

Maximum RF Input Frequency = 5GHz
• 16 DACs @ 6.544GSPS
• 16 ADCs @ 2.275GSPS

3rd Generation
ZU4XDR

Maximum RF Input Frequency > 6GHz
• 8 or 16 DACs @ 16GSPS
• 10 ADCs @ 8GSPS or 20 ADCs @ 4GSPS

Maximum RF Input Frequency = 6GHz
• 8 or 16 DACs @ 10.0GSPS
• 8 ADCs @ 5.0GSPS or 16 ADCs @ 2.5GSPS

4th Generation

All sample rates are maximum

2018 2019 2020 2021
# Zynq UltraScale+ RFSoC Gen 1 Product Table

<table>
<thead>
<tr>
<th>Analog-Digital Signal</th>
<th>ZU21DR</th>
<th>ZU25DR</th>
<th>ZU27DR</th>
<th>ZU28DR</th>
<th>ZU29DR</th>
</tr>
</thead>
<tbody>
<tr>
<td>12-bit, 4.096 GSPS ADC</td>
<td>-</td>
<td>8</td>
<td>8</td>
<td>8</td>
<td>-</td>
</tr>
<tr>
<td>12-bit, 2.058GSPS ADC</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>16</td>
</tr>
<tr>
<td>14-bit, 6.544GSPS DAC</td>
<td>-</td>
<td>8</td>
<td>8</td>
<td>8</td>
<td>16</td>
</tr>
<tr>
<td>SD-FEC</td>
<td>8</td>
<td>-</td>
<td>-</td>
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<tr>
<td>Application Processor Core</td>
<td>Quad-core ARM Cortex-A53 MPCore up to 1.33GHz</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Real-Time Processor Core</td>
<td>Dual-core ARM Cortex-R5 MPCore up to 533MHz</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>High Speed Connectivity</td>
<td>DDR4-2666, PCIe Gen3 x16, 100G Ethernet</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Logic Density (System Logic Cells)</td>
<td>930K</td>
<td>678K</td>
<td>930K</td>
<td>930K</td>
<td>930K</td>
</tr>
<tr>
<td>DSP Slices</td>
<td>4,272</td>
<td>3,145</td>
<td>4,272</td>
<td>4,272</td>
<td>4,272</td>
</tr>
<tr>
<td>33G Transceivers (Max)</td>
<td>16</td>
<td>8</td>
<td>16</td>
<td>16</td>
<td>16</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Packages</th>
<th>ZU21DR</th>
<th>ZU25DR</th>
<th>ZU27DR</th>
<th>ZU28DR</th>
<th>ZU29DR</th>
</tr>
</thead>
<tbody>
<tr>
<td>35mmx35mm</td>
<td>D1156</td>
<td>E1156</td>
<td>E1156</td>
<td>E1156</td>
<td></td>
</tr>
<tr>
<td>40mmx40mm</td>
<td>G1517</td>
<td>G1517</td>
<td>G1517</td>
<td></td>
<td></td>
</tr>
<tr>
<td>42.5mmx42.5mm</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>F1760</td>
</tr>
</tbody>
</table>
Zynq UltraScale+ RFSoC Gen 1 in Production, All Devices Shipping

- All Devices in Production
  - Lidded and Lidless all Available 6 week lead time
- Public Access
  - Vivado & SDK, documented flows
  - Key IP, drivers, RF debug tooling

- ZCU111 Evaluation Kit – Shipping Now
  - Equipped with ZU28DR Production Silicon
  - ZCU111 RF
  - Data Converter Evaluation Tool - Now
    - Evaluate RF Capabilities through Ethernet
    - Multiband configuration management
      - User friendly GUI

- ZCU1275: OOE Sep - Shipping Q1 2019
  - Equipped with ZU29DR Production Silicon
  - Ideal for RF performance analysis
  - Uses RF Analyzer Tool
Zynq UltraScale+ RFSoC Gen 2 Addresses sub-5GHz bands with up to 5 GHz Direct RF Sampling

Wireless

Extended Range with GEN 1 Portfolio

Extended Range with GEN 2

0 1 2 3 4 5 6GHz

- Existing Cellular Bands
- New sub-6GHz 5G Bands

ZU+ Gen 2 address 4.9 GHz international 5G band

> ZU+ XCZU39DR will address 4.9GHz bands in China and Japan
  >> 16T 16R configuration
  >> Available in -2I and -L2I grades.
  >> Same package as XCZU29DR
  >> Samples in March 2019, Production in June 2019
    - Meets time to market needs sub-5GHz LTE bands.
# Zynq UltraScale+ RFSoC Gen 2 Product Table

<table>
<thead>
<tr>
<th>Analog-Digital Signal</th>
<th>Processing System &amp; Programmable Logic</th>
<th>Packages</th>
</tr>
</thead>
<tbody>
<tr>
<td>12-bit, 4.096GSPS ADC</td>
<td>Application Processor Core</td>
<td>35mmx35mm</td>
</tr>
<tr>
<td>12-bit, 2.275GSPS ADC</td>
<td>Real-Time Processor Core</td>
<td>40mmx40mm</td>
</tr>
<tr>
<td>14-bit, 6.544GSPS DAC</td>
<td>High Speed Connectivity</td>
<td>42.5mmx42.5mm</td>
</tr>
<tr>
<td>SD-FEC</td>
<td>Logic Density (System Logic Cells)</td>
<td>F1760</td>
</tr>
<tr>
<td></td>
<td>DSP Slices</td>
<td></td>
</tr>
<tr>
<td></td>
<td>33G Transceivers</td>
<td></td>
</tr>
</tbody>
</table>

## Radio

<table>
<thead>
<tr>
<th></th>
<th>ZU39DR</th>
</tr>
</thead>
<tbody>
<tr>
<td>4.9GHz 5G bands</td>
<td></td>
</tr>
</tbody>
</table>

- **Quad-core ARM Cortex-A53 MPCore up to 1.33GHz**
- **Dual-core ARM Cortex-R5 MPCore up to 533MHz**
- **DDR4-2666, PCIe Gen3 x16, 100G Ethernet**
- **Logic Density (System Logic Cells)**: 930K
- **DSP Slices**: 4,272
- **33G Transceivers**: 16

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<table>
<thead>
<tr>
<th>Packages</th>
</tr>
</thead>
<tbody>
<tr>
<td>35mmx35mm</td>
</tr>
</tbody>
</table>

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*Note: Xilinx Confidential Information*
Introducing 3rd Generation Zynq UltraScale+ RFSoCs
Greater RF Performance – 6GHz of Analog Bandwidth

Wireless
- RF Input with GEN 1 Portfolio
- Extended RF Input with GEN 3
- Existing Cellular Bands
- New sub-6GHz 5G Bands

DAR
- 14-bit Digital-to-Analog Converters
  - 8x @ up to 10.0 GSPS
  - 16x @ up to 10.0 GSPS

ADC
- 14-bit Analog-to-Digital Converters
  - 8x @ up to 2.5 GSPS
  - 16x @ up to 5.0 GSPS

Radar
- RF Input with GEN 1 Portfolio
- Extended RF Input with GEN 3
- L-Band
- S-Band
- C-Band
# Zynq UltraScale+ RFSoC Gen 3 Product Table

<table>
<thead>
<tr>
<th>Analogue-Digital Signal</th>
<th>Radio</th>
<th>Radar / Fixed Wireless</th>
<th>Backhaul</th>
<th>Radar / Fixed Wireless</th>
</tr>
</thead>
<tbody>
<tr>
<td>14-bit, 5.0GSPS ADC</td>
<td>ZU45DR</td>
<td>ZU46DR</td>
<td>ZU47DR</td>
<td>ZU48DR</td>
</tr>
<tr>
<td>14-bit, 2.5GSPS ADC</td>
<td>–</td>
<td>8</td>
<td>–</td>
<td>8</td>
</tr>
<tr>
<td>14-bit, 10GSPS DAC</td>
<td>4</td>
<td>12</td>
<td>–</td>
<td>8</td>
</tr>
<tr>
<td>SD-FEC</td>
<td>–</td>
<td>8</td>
<td>–</td>
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<td>16</td>
</tr>
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<th>Backhaul</th>
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<td>H1760</td>
<td></td>
<td></td>
<td>F1760</td>
</tr>
</tbody>
</table>
## Scalability Across the Portfolio

### Radio

- Gen 1
- Gen 2
- Gen 3

### Backhaul

- Gen 1
- Gen 2
- Gen 3

### Baseband

- Gen 1
- Gen 2
- Gen 3

### Fixed Wireless Access

- Gen 1
- Gen 2
- Gen 3

### Cable R-PHY

- Gen 1
- Gen 2
- Gen 3

### Radar / SIGINT

- Gen 1
- Gen 2
- Gen 3

<table>
<thead>
<tr>
<th>Subsystem</th>
<th>ZU21DR</th>
<th>ZU25DR</th>
<th>ZU27DR</th>
<th>ZU28DR</th>
<th>ZU29DR</th>
<th>ZU39DR</th>
<th>ZU45DR</th>
<th>ZU46DR</th>
<th>ZU47DR</th>
<th>ZU48DR</th>
<th>ZU49DR</th>
</tr>
</thead>
<tbody>
<tr>
<td>RF-ADC w/DDC</td>
<td>-</td>
<td>8</td>
<td>8</td>
<td>8</td>
<td>16</td>
<td>16</td>
<td>4</td>
<td>8</td>
<td>4</td>
<td>8</td>
<td>8</td>
</tr>
<tr>
<td>Max ADC rate (GSPP)</td>
<td>-</td>
<td>4.096</td>
<td>4.096</td>
<td>4.096</td>
<td>2.058</td>
<td>2.275</td>
<td>5.0</td>
<td>2.5</td>
<td>5.0</td>
<td>5.0</td>
<td>5.0</td>
</tr>
<tr>
<td>Resolution (bits)</td>
<td>-</td>
<td>12</td>
<td>12</td>
<td>12</td>
<td>12</td>
<td>12</td>
<td>14</td>
<td>14</td>
<td>14</td>
<td>14</td>
<td>14</td>
</tr>
<tr>
<td># of ADCs</td>
<td>-</td>
<td>8</td>
<td>8</td>
<td>8</td>
<td>16</td>
<td>16</td>
<td>4</td>
<td>12</td>
<td>8</td>
<td>8</td>
<td>16</td>
</tr>
<tr>
<td>Max DAC Rate (GSPP)</td>
<td>-</td>
<td>6.544</td>
<td>6.544</td>
<td>6.544</td>
<td>6.544</td>
<td>6.544</td>
<td>10.0</td>
<td>10.0</td>
<td>10.0</td>
<td>10.0</td>
<td>10.0</td>
</tr>
<tr>
<td>Resolution (bits)</td>
<td>-</td>
<td>14</td>
<td>14</td>
<td>14</td>
<td>14</td>
<td>14</td>
<td>14</td>
<td>14</td>
<td>14</td>
<td>14</td>
<td>14</td>
</tr>
<tr>
<td>SD-FEC</td>
<td>8</td>
<td>-</td>
<td>-</td>
<td>8</td>
<td>-</td>
<td>-</td>
<td>8</td>
<td>-</td>
<td>8</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>RF input Freq max. GHz</td>
<td>4</td>
<td>-</td>
<td>-</td>
<td>4</td>
<td>-</td>
<td>-</td>
<td>5</td>
<td>-</td>
<td>6</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Decimation / Interpolation</td>
<td>1x, 2x, 4x, 8x</td>
<td>1x, 2x, 4x, 8x</td>
<td>1x, 2x, 4x, 8x</td>
<td>1x, 2x, 4x, 8x</td>
<td>1x, 2x, 4x, 8x</td>
<td>1x, 2x, 4x, 8x</td>
<td>1x, 2x, 4x, 8x</td>
<td>1x, 2x, 4x, 8x</td>
<td>1x, 2x, 4x, 8x</td>
<td>1x, 2x, 4x, 8x</td>
<td>1x, 2x, 4x, 8x</td>
</tr>
<tr>
<td>System Logic Cells (K)</td>
<td>930</td>
<td>678</td>
<td>930</td>
<td>930</td>
<td>930</td>
<td>930</td>
<td>678</td>
<td>930</td>
<td>930</td>
<td>930</td>
<td>930</td>
</tr>
<tr>
<td>DSP Slices</td>
<td>4,272</td>
<td>3,145</td>
<td>4,272</td>
<td>4,272</td>
<td>4,272</td>
<td>4,272</td>
<td>4,272</td>
<td>4,272</td>
<td>4,272</td>
<td>4,272</td>
<td>4,272</td>
</tr>
<tr>
<td>GTY Transceivers</td>
<td>16</td>
<td>8</td>
<td>16</td>
<td>16</td>
<td>16</td>
<td>16</td>
<td>8</td>
<td>16</td>
<td>16</td>
<td>16</td>
<td>16</td>
</tr>
<tr>
<td>PCIe® Gen 3x16</td>
<td>2</td>
<td>1</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>1</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>100G Ethernet w/RS-FEC</td>
<td>2</td>
<td>1</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>1</td>
<td>2</td>
<td>2</td>
<td>2</td>
</tr>
</tbody>
</table>

### Package Footprint

<table>
<thead>
<tr>
<th>Package Footprint</th>
<th>ZU21DR</th>
<th>ZU25DR</th>
<th>ZU27DR</th>
<th>ZU28DR</th>
<th>ZU29DR</th>
<th>ZU39DR</th>
<th>ZU45DR</th>
<th>ZU46DR</th>
<th>ZU47DR</th>
<th>ZU48DR</th>
<th>ZU49DR</th>
</tr>
</thead>
<tbody>
<tr>
<td>D1156</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>E1156</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>G1517</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>F1760</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>H1760</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Integrated IP</th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>D1156</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>E1156</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>G1517</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>F1760</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>H1760</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Adaptable.
Intelligent.